PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Teck Kheng Lee

Serial No.: 10/782,270

Filed: February 18, 2004

For: INTERPOSER SUBSTRATE AND WAFER SCALE INTERPOSER SUBSTRATE MEMBER FOR USE WITH FLIP-CHIP CONFIGURED SEMICONDUCTOR DICE

Confirmation No.: 4215

Examiner: J. Clark

Group Art Unit: 2815

Attorney Docket No.: 2269-4973.1US
(00-0593.01/US)

CERTIFICATE OF MAILING

I hereby certify that this correspondence along with any attachments referred to or identified as being attached or enclosed is being deposited with the United States Postal Service as First Class Mail on the date of deposit shown below with sufficient postage and in an envelope addressed to the Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

December 21, 2004
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Joseph A. Walkowski
Name (Type/Print)

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In compliance with the duty to disclose information material to patentability pursuant to 37 C.F.R. § 1.56, it is respectfully requested that this Supplemental Information Disclosure Statement be entered and the documents listed on attached Form PTO-1449 or PTO/SB/08 be considered by the Examiner and made of record. Copies of U.S. patents are not being submitted pursuant to M.P.E.P. 609 III A(2). Copies of foreign patent documents and non-patent literature are enclosed pursuant to 37 C.F.R. § 1.98(a)(2).

In accordance with 37 C.F.R. § 1.97(g) and (h), filing of this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made or an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b). Further, no representation is made by Applicant herein that no other possible material information as defined in 37 C.F.R. § 1.56 (b) exists.

U.S. Patent Documents

U.S. Patent No.	Publication Date	Patentee
US - 3,239,496	03/1966	Jursich
US - 4,074,342	02/1978	Honn et al.
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US - 5,148,265	09/1992	Khandros
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Document No.	Publication Date	Patentee
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EP 1009027	06/2000	Okuno
KR 2001054744	07/2001	Choi et al. (English Abstract)

Other Documents

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GEISSINGER et al., "Tape Based CSP Package Supports Fine Pitch Wirebonding," *Electronics Manufacturing Technology Symposium*, 2002, IEMT 2002, 27th Annual IEEE/SEMI International, 17-18 July 2002, pp. 41-452.

HATANAKA, H., "Packaging processes using flip chip bonder and future directions of

Other Documents

technology development," *Electronics Packaging Technology Conference*, 2002. 4th, 10-12, Dec. 2002, pp. 434-439.

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LYONS et al., "A New Approach to Using Anisotropically Conductive Adhesives for Flip-Chip Assembly, Part A, " *IEEE Transactions on Components, Packaging, and Manufacturing Technology,* Vol. 19, Issue 1, March 1996, pp. 5-11.

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TEUTSCH et al, "Wafer Level CSP using Low Cost Electroless Redistribution Layer," *Electronic Components and Technology Conference*, 2000. 2000 Proceedings. 50th, 21-24 May 2000, pp. Pages: 107-113.

"The 2003 International Technology Roadmap for Semiconductor: Assembly and Packaging."

TSUI et al., "Pad redistribution technology for flip chip applications," *Electronic Components and Technology Conference*, 1998. 48th IEEE, 25-28 May 1998, pp. 1098-1102.

XIAO et al., "Reliability study and failure analysis of fine pitch solder-bumped flip chip on low-cost flexible substrate without using stiffener," IEEE, 2002. Proceedings 52nd, 28-31 May 2002, pp. 112-118.

Australian Search Report dated 11 Aug 2004 (3 pages).

Australian Search Report dated 16 Aug 2004 (4 pages).

Applicant offers to supply any explanation or discussion of the documents which the Examiner feels is necessary or desirable and which is requested.

This Supplemental Information Disclosure Statement is filed after the mailing date of the first Office Action on the merits.

The fee pursuant to 37 C.F.R. § 1.17(p) is enclosed.

Respectfully submitted,

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Date: November 24, 2004
JAW/lmh:ljb
Enclosures: Form PTO-1449 or PTO/SB/08
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 4

Complete if Known	
Application Number	10/782,270
Filing Date	February 18, 2004
First Named Inventor	Teck Kheng Lee
Group Art Unit	2815
Examiner Name	J. Clark
Attorney Docket Number	2269-4973.1US (00-0593.01/US)

U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No.[1]	Document Number Number - Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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		EP 684644	11/1995	Kata et al.		
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		EP 1009027	06/2000	Okuno		
		KR 2001054744	07/2001	Choi et al. (English Abstract)		x

Examiner Signature		Date Considered	

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Sheet 3 of 4

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		AL-SARAWI et al., "A review of 3-D packaging technology," *Components, Packaging, and Manufacturing Technology, Part B: IEEE Transactions on Advanced Packaging*, Vol 21, Issue 1, Feb. 1998, pp. 2-14.	
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		US- 6,034,427	03/07/2000	Lan et al.	
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PATENT & TRADEMARK OFFICE MAILROOM DATE STAMPED HEREON IS AN ACKNOWLEDGEMENT THAT ON THIS DATE THE PATENT & TRADEMARK OFFICE RECEIVED:

Supplemental Information Disclosure Statement (2 pages); and Form PTO/SB/08 (1 page), with copy of cited references (3 documents)

Invention:	INTERPOSER SUBSTRATE AND WAFER SCALE INTERPOSER SUBSTRATE MEMBER FOR USE WITH FLIP-CHIP CONFIGURED SEMICONDUCTOR DICE
Applicant(s):	Teck Kheng Lee
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Date Sent:	April 22, 2004 via first class mail
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JAW/ps:ljb